REMARKS

In view of the following remarks and the foregoing amendments, reconsideration and allowance are respectfully requested.

Claims 1-19 are pending at the time of this action, with Claims 1, 3-6, 12, 16 and 18 being independent. Claims 1-15, 18 and 19 are allowed.

Claims 16 stands rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Pettijohn et al (US Patent 5,149,954). Claim 17 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Pettijohn. These contentions are respectfully traversed.

35 U.S.C. 102 – Claim 16

Amended Claim 16 is patentable over Pettijohn at least because Pettijohn fails to disclose each and every feature of the claim. For example, Pettijohn fails to disclose the feature of "wherein the linear integrator array of switched-capacitor integrators are **arranged in rows and columns respectively equal to rows and columns of said linear sensing array**," as recited in the claim. The amendments to Claim 16 are not new matter and similar to the patentable features in allowed Claim 1.

Pettijohn discloses techniques for performing time delay and integration (TDI) in switched-capacitor circuits (Pettijohn: Abstract). Pettijohn discloses a first step of storing an electrical signal on a capacitor in a radiation detector array 2, where the detector array 2 has detectors, coupling capacitors 4, and source follower amplifiers 5 (Pettijohn: Abstract; Col. 3, lines 3-11, 23-26, 43-45). Pettijohn discloses a second step of using a TDI circuit 1 to equilibrate the stored charge in one time sample with a stored charge in a subsequent time sample by shorting storage capacitors (e.g., C1, C2, C3) together to sum coherent signals (Pettijohn: Abstract; Fig. 1a, 2; Col. 3, lines 49-68; Col. 4, lines 1-27, 43-51). The TDI circuit 1 then sends the equilibrated (summed) signal onto other stages for processing (Pettijohn: Figs. 1c, 2, 3; Col. 4, lines 9-17). Pettijohn discloses that **the linear sensing array (i.e., the radiation detector array 2** in Figs. 1a, 1c, 3) has switched-capacitor circuits arranged in rows and columns in Figs. 1a, 1c, 3. However, Pettijohn fails to disclose a "linear integrator array of switched-capacitor integrators are **arranged in rows and columns respectively equal to rows and columns of said**

linear sensing array" (emphasis added). In contrast, Pettijohn shows a switched-capacitor sensing circuit for every detector signal (V_A, V_B) in the linear sensing array (i.e., the radiation detector array 2 in Fig. 1a), and a TDI circuit that has a summing capacitor (C1, C2, C3, C4, C5) for every clock interval in the TDI array (i.e., clock interval Φ1 for C1, clock interval Φ2 for C2, clock interval Φ3 for C3, clock interval Φ4 for C4, clock interval Φ5 for C5) (Pettijohn: Figs. 1a, 3; Col. 3, lines 49-68; Col. 4, lines 1-42; see e.g., "it can be seen that the TDI circuit of the invention employs sample and hold capacitors in conjunction with proper clock phasing to provide a temporal memory to realize the TDI function," Col. 4, lines 43-46). Pettijohn relies on the clock phasing to provide the TDI function and is silent about disclosing the claimed equivalence between the row and columns of the linear sensing array and the linear integrator array. Hence, the burden to establish anticipation has not been met at least because Pettijohn fails to disclose each and every feature of the claim under consideration.

Furthermore, Pettijohn fails to disclose the claim features of the "one-to-one mapping relationship," as recited in Claim 16. For example, since Pettijohn fails to disclose a "linear integrator array of switched-capacitor integrators ... arranged in rows and columns respectively equal to rows and columns of said linear sensing array," Pettijohn fails to disclose a one-to-one mapping relationship for each sensor/detector with a respective (disparate) integrator for each pixel in each column (see e.g., Instant Disclosure: Fig. 1C, page 11, lines 12-14). For at least this reason, Pettijohn also fails to disclose the Claim 16 features of "wherein for each frame, pixels in columns of the linear sensing array are mapped **in a one-to-one mapping relationship** to switched-capacitor integrators in respective columns in the linear integrator array" (emphasis added). Instead of disclosing a one-to-one mapping relationship, Pettijohn shows that multiple sensors/detectors (e.g., Pettijohn: Fig. 1a, detector for V_A, V_B, etc.) in the detector array 2 are connected to a TDI circuit 1 in a column generally (see e.g., Pettijohn: Figs. 1a, 1c, 3). Since Pettijohn fails to disclose a one-to-one mapping relationship as recited in the claim, the rejection to Claim 16 under 35 U.S.C. 102 should be withdrawn, and Claim 16 should be placed in condition for allowance.

35 U.S.C. 103 – Claim 17

Claim 17 is patentable for at least depending upon an allowable base claim (base Claim 16), as well as for reciting patentable subject matter in its own right.

Conclusion

In view of the amendments and remarks herein, the Applicants believe that Claims 1-19 are in condition for allowance and ask that these pending claims be allowed. The foregoing comments made with respect to the positions taken by the Examiner are not to be construed as acquiescence with other positions of the Examiner that have not been explicitly contested. Accordingly, the arguments for patentability of a claim should not be construed as implying that there are not other valid reasons for patentability of that claim or other claims.

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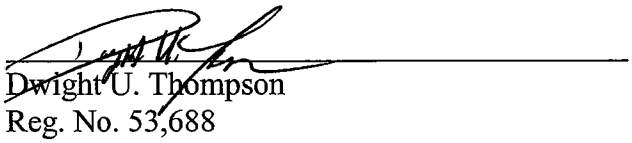
Respectfully submitted,

Date: Oct. 3, 2006



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